REMARKS

Rejections Under 35 U.S.C. §112

Claims 1-8 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 1, 6, and 8 have been amended to fix a typographical error. The method now identifies an address of a memory cell that is greater than the lowest address *in* the selected addressable block.

The Examiner noted that claims 3-5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. §112, second paragraph, as set forth in the Office Action and to include the limitations of the base claim and any intervening claims.

Rejections Under 35 U.S.C. §102

Claims 1-2 and 6-8 were rejected under 35 U.S.C. §102(b) as being anticipated by *Honda et al.* (U.S. Patent 6,377,502). Applicant respectfully traverses this rejection.

Honda et al. discloses a memory cell array 1 that has a plurality of cores (0 – m-1), each core comprising a block or a set of a plurality of blocks defining a range of memory cells. The Examiner states that "a core block register 42 is used to hold information of which block in the core is written or erased". However, at column 13, lines 5 – 10 of *Honda et al.*, it is stated that "[t]he data write signal WRITE or erase signal ERASE obtained by decoding a command in the interface circuit 14 is held as information indicating which block in the core has been selected for write or erase, in a core block register 42..." This clearly states that the core block register 42 holds information for blocks that have been selected to be erased, not the blocks that have already been erased and require verification. Therefore, the Examiner's equating of Applicant's claimed erase indication register with the core block register 42 of *Honda et al.* is in error since blocks selected to be erased do not yet require erase verification.

Additionally, *Honda et al.* neither teaches nor suggests Applicant's claimed method for performing an erase verification on a memory array. In fact, the only portion of *Honda et al.* that discusses a verifying an erase is column 10, lines 42 – 47. This passage states that when the erase operation is complete, the data is detected by a sense amplifier circuit and, if the erase is sufficient, the operation is completed. If the erase

operation is insufficient, an additional erase is performed. This is not an erase verification method as claimed by Applicant of selecting an addressable memory block, identifying the lowest address within the memory block, and performing an erase verification on that address.

CONCLUSION

Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact the under-signed at (612) 312-2200. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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